

Los Angeles, CA 90036-5679

United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FII	LING DATE		FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,025	0	9/15/2003		Jia-Fam Wong	B-4212DIV 621223-1 2539	
7	590	06/29/2005			EXAMINER	
Richard P. Be	rd P. Berg Gebremariam, samuei			M, SAMUEL A		
Suite 2100	1711111				ART UNIT	PAPER NUMBER
5670 Wilshire	Bouleva	rd			2811	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)	R							
	10/663,025	WONG, JIA-FAM	,,							
Office Action Summary	Examiner	Art Unit								
	Samuel A. Gebremariam	2811								
The MAILING DATE of this communication apperent of the Period for Reply	ears on the cover sheet with the	correspondence add	iress							
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).										
Status										
1) Responsive to communication(s) filed on 22 Ap	<u>oril 2005</u> .	•								
2a) ☐ This action is FINAL. 2b) ☑ This	action is non-final.									
3) Since this application is in condition for allowance except for formal matters, prosecution as to the ments is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.										
Disposition of Claims										
4) ⊠ Claim(s) 18-20 and 26-36 is/are pending in the application. 4a) Of the above claim(s) 18-20 and 26-28 is/are withdrawn from consideration. 5) □ Claim(s) is/are allowed. 6) ⊠ Claim(s) 29-36 is/are rejected. 7) □ Claim(s) is/are objected to. 8) □ Claim(s) are subject to restriction and/or election requirement.										
Application Papers										
9) The specification is objected to by the Examiner	•									
10) ☐ The drawing(s) filed on is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.										
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).										
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d). 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.										
Priority under 35 U.S.C. § 119										
12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 09/884,286. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received.										
• •	·									
Attachment(s)										
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9/15/03.	4) Interview Summary Paper No(s)/Mail D 5) Notice of Informal F 6) Other:	ate	152)							

Application/Control Number: 10/663,025 Page 2

Art Unit: 2811

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of group II, claims 29-36 drawn to a semiconductor device is acknowledged.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 29 and 33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claimed limitation of "the thickness of the first and second sacrifice layers varies according to the thickness of the semiconductor layer because the time for etching the first and second sacrifice layers is substantially equal to the time for etching the semiconductor layer in the subsequent process" as recited in claims 29 and 33 is not clear as to the thickness of the sacrifice layer.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.
- 4. Claims 29-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Sah, US patent No. 6,218,221.

Regarding claims 29 and 33, Sah teaches (fig. 8A) a thin film transistor (TFT), comprising: a gate electrode (42) with an island shape formed on a substrate (40); an insulating layer (44) covering the gate electrode; a semiconductor layer (46) with an island shape formed on the insulating layer (44), and positioned directly above the gate electrode; a source doped silicon layer (46a) and a drain doped silicon layer (46a) formed on the semiconductor layer (46), a channel (region between the two 46a's) being defined between the source doped silicon layer and the drain doped silicon layer to expose the semiconductor layer therein (refer to fig. 8a); first and second sacrifice layers (48a) with island shapes respectively formed on the source doped silicon layer and drain doped silicon layer (refer to fig. 8a), the first and the second sacrifice layers being spaced apart by the channel (fig. 8a); a source electrode (48b) formed above the first sacrifice layer, and the source dope silicon layer (46a); and a drain electrode (48b) formed above the second sacrifice layer (48a) and the drain doped silicon layer (46a). Furthermore Sah teaches that the thickness of the first and second sacrifice layers (48a) varies according to the thickness of the semiconductor layer (46) because the time for etching the first and second sacrifice layers is substantially equal to the time for etching the semiconductor layer in the subsequent process.

Regarding claims 30-31 and 34-35, Sah teaches the entire claimed structure of claims 29 and 33 above including a passivation layer (52) covering the source electrode (48b), the drain electrode (48b), and the channel.

The limitation of "during the etching process, the etching rate of the first and the second sacrifice layers is RIS, the etching rate and the thickness of the drain doped

Art Unit: 2811

silicon and the source doped silicon layers are Rn and Tn, and the etching rate and the thickness of the semiconductor layer are Ra and Ta, and the thickness of the first and the second sacrifice layers TIS meets the equation of (TIS/RIS + Tn/Rn) Y (Tn/K + Ta/Ra)" as recited in claims 30 and 34 is considered a product-by-process claim.

"[E]ven though product-by process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." *In re Thorpe*, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

The limitation of "the TFT is used in an in-plane-switch (IPS) type LCD" is not given patentable weight because a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). Furthermore the structure of Sah can be used as in an in-plane-switch (IPS) type LCD.

Regarding claims 32 and 36, Sah teaches the entire claimed structure of claims 29 and 33 above including a passivation layer (52) covering the TFT on the substrate (40), and having a hole (56) above the drain electrode (48b); and a transparent

Application/Control Number: 10/663,025 Page 5

Art Unit: 2811

conductive layer (54) formed above the drain electrode (48b) and electrically connected to the drain electrode via the hole (refer to fig. 8A).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG June 24, 2005

Steven Loke